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EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/033,027	SNYDER, WARREN	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-18,20,21,23-49,51,52 and 57-59* is/are pending in the application.

4a) Of the above claim(s) *12,19,22,50 and 53-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-18,20,21,23-49,51,52 and 57-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/27/03,04/11/05,03/03/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-11, 13-18, 20,21, 23-49, 51-52, 57, 58,59 are presented for examination. Claims 12, 19, 22, 50, 53-56 have been canceled.

2. Claims 1;11 are objected to because of the following informalities: The language "plurality of functionalities" seems to mean "plurality of functional units", or the like. Appropriate correction is required.

3. Claims 1-11,13-18,20,21,23-49,51,52, 57-59 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: The connection between the digital blocks themselves are not being clearly recited. The claims only recites the digital functional blocks coupled to the interconnect (e.g. see claims 1, 11, 17, see digital blocks coupled to the input and output bocks in claim 35, see digital blocks coupled to the analog blocks in claim 37, see routing matrix coupled the analog blocks to the subsets of digital blocks in claim 42) . The connection between the digital circuit (components) and analog circuit (components) is not clear (see claims 51,52).

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct

from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 42 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,724,220. Although the conflicting claims are not identical, they are not patentably distinct from each other because although patented claim 1 did not recite the single write operation, the patented claim 1 also taught the programmable analog and digital function blocks (see claim 1, lines 1-6). Since programmable had to be done in program instruction, such as the read and write commands), and since no specific type of write instruction ahs been reflected into the pending claim 1, it would have been obvious to one of ordinary skill in the art to recognize that a program instruction, such as write , or read , could also be applicable in the patented claim in order to provide interactive R/W function (e.g. programming), and in doing , provided a motivation.

5. Claim 35 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 8 of U.S. Patent No. 6,724,220. Although the conflicting claims are not identical, they are not patentably distinct from each other

because although patented claim 8 did not recite the single write operation, nor the programmable non-volatile memory as clamed , the patented claim 8 also taught the programmable analog and digital function blocks . Since programmable had to be done in program instruction, such as the read and write commands, and since no specific type of write instruction has been reflected into the pending claim 8, it would have been obvious to one of ordinary skill in the art to recognize that a program instruction, such as write , or read , could also be applicable in the patented claim in order to enhance the user interface capability (e.g. programming), and in doing , provided a motivation. As to the programmable non-volatile memory, the examiner holds since the specific type of non-volatile memory ahs been recited in the claim, it would have been recognizable the use of non-volatile memory in general.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,37,52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzori (5,748,875) in view of Insenser Farre et al. (6,460,172) .

a) a bus (fig.1, [pod 32]);

b) a microprocessor [CPU 44] coupled to the bus (see fig.1 [44]);

c) a memory [52] coupled to said bus [pod 32]; and

d) a plurality of functionalities (see fig.1 [36] [42] [34] coupled to the bus [32] , non-volatile memory functions to program the functionalities (see RAM 52 contained program to configure the digital blocks 36 in col.8, lines 45-55)

e) an interconnect (fig.1, 42, 278) dynamically configurable and programmable;

f) a dynamically configurable and programmable digital functional block (36a, 36b) coupled to the interconnect [42,278], the digital functional block configurable to perform any one of a plurality of digital functions (see digital function blocks in col.8, lines 24-67, see also the configuration data loaded into the digital blocks 36 in col.9, lines 1-42).

7. As to the single register write operation (see loading of the configuration data in col.9, lines 30-42). A load is a register write operation.

8. Tzori did not specifically sow the analog function blocks as claimed. However, Insenser taught analog blocks (see fig.1 [4]), and were "programmable" and many functional parameters could be "configurable" (see col.4, lines 40-42). It would have been obvious to one of ordinary skill in the art to use Insenser in Tzori for including the analog blocks as clamed because the use of Insenser could provide the ability of Tzory for accepting extended functional blocks of different type, and it could be done by predefining the analog blocks of Insenser into the configuration file of Tzory (e.g. see logic configuration library [86] of Tzori in fig.1) with modified control read and write port parameters , so that specific analog blocks of Insenser could be recognized by Tzory,

and because Tzory also taught to adapt interfacing between various different types of IC's and a digital logic computer simulation (see col.4, lines 26-29), which was a suggestion of the applicability of functional IC's different than digital function block , such as analog functional units, and for the above reason , provided a motivation.

9. As to the programmable non-volatile memory, the examiner holds since the specific type of non-volatile memory ahs been recited in the claim, it would have been recognizable the use of non-volatile memory in general.

10. As to claim 52, Tzori taught :

a) a microcontroller comprising a memory (see fig..1 [52]);

b) a subsystem (see fig.1 [32] comprising an array of digital components [36a][36b], and the digital components are programmed with code stored in the memory [52] (see RAM 52 contained program to configure the digital blocks 36 in col.8, lines 45-55), each digital component was configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation (see configurable digital blocks 36a,b by the programming in col.8, lines 24-56, see also the loading of the configuration data in col.9, lines 31-42 for the write operation); and

c) a coupling mechanism [fig.1 [24] [66]] coupled to the subsystem [32]; selectively, functionality is configurable to execute a first function (digital function) according to an input of a first type (see configuration input data in col.9, lines 31-35), and implemented a connectability state for the system with which the system is connectable to an external entity (see [fig.1 [28][86][232]] according to a user input of a second type [26].

Tzori did not specifically sow the analog function blocks as claimed. However, Insenser taught analog blocks (see fig.1 [4]), and were "programmable" and many functional parameters could be "configurable" (see col.4, lines 40-42). The reasons of obviousness were already given in paragraph above, therefore, it will not be repeated herein.

11. Claims 1-11,13-18,20,21,23-49,51,52, 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al. (6,460,172) in view of Furtek (5,894,565) in view of van der Wal et al. (6,188,381).

12. As to the feature of "microcontroller" in claim 1, Insenser Farre et also included micro controller (see fig.1 (2)).

13. As to the remaining limitations in claim 1, Insenser Farre et. also disclosed a circuit (FIPSOC) (see fig.1) comprising at least :

a) a bus (9);

b) a microprocessor coupled to the bus (not explicitly shown in the figure, but taught in col.2, lines 40-51, col.3, lines 22-24 as on-chip microprocessor;

c) memory (see fig.1 [1]) :

a plurality of functionalities (fig.1 (3)(4)). Comprising

1) interconnect (see the connection to (3) and (4)),

2) analog circuit (fig.1 [4]);

3) a digital functional block to the interconnect (see fig.1(3)).

14. As to the feature of non-volatile memory functions to program the functionalities Insenser did not specifically showed the non-volatile memory as claimed. However, Furtek disclosed a non-volatile memory to program the functionalities (see col.12, lines 3-6). It would have been obvious to one of ordinary skill in the art to use Furtek in Insenser for including the non- volatile memory as claimed because the use of Furtek could provide Insenser the ability to adapt to different type of memory storage, and therefore, increasing the storage adaptability of Insenser, and it could be readily achieved by predefining the control parameters of the non-volatile memory of Furtek , such as the memory type and word width, into Insenser so that the non-volatile memory of Furtek could be recognized by Insenser in order to enhance the storage adaptability, and for the above reason provided a motivation.

15. As to the feature of the analog functional block is dynamically configurable and programmable, Insenser clearly taught his analog blocks was "programmable" and many functional parameters could be "configurable" (see col.4, lines 40-42). The fixed functionality blocks were directed to the functionality blocks of coarse granularity, and it did not mean that Insensers analog functional blocks were not programmable and non-configurable.

16. As to the dynamically configurable and programmable digital block, Insensers digital black was also dynamically configurable and programmable (see programmable

digital cells in col.3, lines 15-19, see the microprocessor was used to reconfigure the cells in col.3, lines 45-46).

17. As to the feature of dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, Insensers digital black was also dynamically configurable and programmable (see programmable digital cells in col.3, lines 15-19, see the microprocessor was used to reconfigure the cells in col.3, lines 45-46), and also taught his microprocessor used for both controlling and configuring the whole system and running general purpose user program and optimized interfaces between these three blocks that would allow the user to read digital signals implemented in the programmable logic array as memory array in real time, directly interface the digital part of the analog and digital signals from microprocessor and from the programmable logic, and configurable and dynamically reconfigure all the programmable features of the system with the microprocessor between countless other possibilities (see col.2, lines 4-10). Therefore, Insensers was also configurable to perform any functions .

18. As to the feature of digital functional block configurable to perform any function upon being configured with a single register write operation, Insensers was also configurable to perform any functions (see discussions above) . Insensers did not specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). art would have been obvious

to one of ordinary skill in the art to use van der Wal in Insensers for reconfiguring the digital functions with a single register write operation as claimed because the use of van der Wal could provide Insensers the ability to control the reconfigurable function blocks in a single integrated format, therefore, reducing the hardware circuit overheads, and it could be achieved by predefining the single register write of van der Wal into eh configuration file of Insensers with modified control variables (e.g. the instruction format, the write length etc.) so that the single register write of van der Wal could be recognized by Insensers, and because Insensers also taught a single microprocessor command for reconfiguring the SOC system (see col.5, lines 1-9), which was a suggestion of the applicability of a single register write operation in order to achieve specific register access operation for reconfiguring purpose, and for doing so, provided motivation.

19. As to the teaching of van der Wal 's single control register write for switching all bits of the video data in all devices simultaneously, the switching itself was a reconfiguring function, such as, on and off configurations, therefore, the single write in van der Wal was directed to the reconfiguring of all functional blocks (or all the devices, see col.10, lines 30-38).

20. As to the function taught in pages 27,28, and 44-45 of applicant's specification, applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). The specific analog and digital functions in the specification are not being reflected into the claims

21. As to claims 3, 4, Insenser also included programmable 1/0 (see fig.1 [5], col.3, lines 18-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks).

22. As to claims 5,6, Insenser also included analog functional block (4) and digital functional block (4) (see fig.1 , col.1, lines 15-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks).

3. As to claim 7, Insenser also included configuration state (see also col.2, lines 1-14 for background teaching of programmable configuring and reconfiguring features of logic blocks, see the configuration contexts in col.4, lines 1-7).

23. As to claim 8, see the CAD tools in fig.4 for user input.

24. As to claims 9,10,23,24, although Insenser disclosed a RAM (1), it did not show a read only memory (claim 9) or erasable memory (claim 23) as claimed. However Furtek disclosed a erasable read only memory (EPROM, electrically erasable programmable rom) in a logic circuit cell (see col.1 , lines 20-28). It would have been obvious to one of ordinary skill in the ad to use Furtek in Insenser for including the read only memory as claimed because the use of Furtek could provide Insenser a greater storage capability to adapt to specific access format of a given type of memory, such as the read only, and because Furtek already taught the read only memory being used in programmable integrated logic circuit blocks, one of ordinary skill in the art should be

able to recognize the advantages of adding read only memory into Insenser's circuit block for the expanded storage structure compatibility, and for the above reason, provided a motivation.

25. As to the feature of "microcontroller" and the "non-volatile memory" in claim 11 , Insenser taught micro controller (see fig.1 (2)). Insenser did not specifically showed the non-volatile memory as claimed. However, Furtek disclosed a non-volatile memory (see col.12, lines 3-6). It would have been obvious to one of ordinary skill in the ad to use Furtek in Insenser for including the non-volatile memory as claimed because the use of Furtek could provide Insenser the ability to adapt to different type of memory storage, and therefore, increasing the storage adaptability of Insenser, and it could be readily achieved by predefining the control parameters of the non-volatile memory of Furtek , such as the memory type and word width, into Insenser so that the non-volatile memory of Furtek could be recognized by Insenser in order to enhance the storage adaptability, and for the above reason provided a motivation.

26. As to remaining limitations of claim 11, Insenser taught at least :

a) a bus (9) ;

b) a microprocessor coupled to the bus (not explicitly shown in the figure, but taught in col.2, lines 40-51 , col.3, lines 22-24 as on-chip microprocessor;

c) memory (1) :

a plurality of functionalities ((3)(4)). Comprising

1) interconnect (see the connection to (3) and (4))..,

2) analog circuit ((4))..,

3) a digital functional block to the interconnect (see fig.1(3));

d) programmable 1/0 (see fig.1 (5), col.3, lines 18-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks;

e) analog functional block (4) and digital functional block 14) (see fig.1, col.1, lines 15-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks).

27. As to the feature of the analog functional block is dynamically configurable and programmable to perform various functions, Insenser clearly taught his analog blocks was "programmable" and many functional parameters (i.e. the analog functions) could be "configurable" (see col.4, lines 40-42). The fixed functionality blocks were directed to the functionality blocks of coarse granularity, and it did not mean that Insensers analog functional blocks were not programmable and non- configurable.

28. As to the dynamically configurable and programmable digital block, Insensers digital black was also dynamically configurable and programmable (see programmable digital cells in col.3, lines 15-19, see the microprocessor was used to reconfigure the cells in col.3, lines 45-46).

29. As to the single register write operation, neither Insensers nor Furtek specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). See reasons for obviousness set forth above.

30. As to claim 13, 14, Insenser also included user input (see the high level language HDL, in col.2, lines 27-39, see also col.5, lines 4-6).

31. As to claim 15, Insenser also included configuration state (see also col.2, lines 1-14 for background teaching of programmable configuring and reconfiguring features of logic blocks, see the configuration contexts in col.4, lines 1-7).

32. As to claim 16, see the high level language HDL, in col.2, lines 27-39, see also col.5, lines 4-6).

33. As to the feature of "microcontroller " in claim 17, Insenser taught micro controller (see fig.1 (2)).

34. As to the " programmable non-volatile memory coupled to the digital blocks and analog blocks for programming " in claim 17, Insenser did not specifically showed the programmable non-volatile memory' coupled to his digital and analog blocks for programming as claimed. . However, Furtek disclosed a non-volatile memory 83 which included a write enable signal (see col.12, lines 3-24). Therefore, it can be seen that the non-volatile memory 83 was writable for programming, and therefore, it was programmable. Furtek also disclosed that the programmable gate arrays typically employ non-volatile memory cell technology for configuration by user (see col.1, lines 19-36) . Therefore, the non-volatile memory cell had to be programmable for configuration by the user. It would have been obvious to one of ordinary skill in the art

to use Furtek in Insenser for including the programmable non-volatile memory as claimed because the use of Furtek could provide Insenser the ability to adapt to different type of memory storage, and therefore, increasing the storage adaptability of Insenser, and it could be readily achieved by predefining the control parameters of the non-volatile memory of Furtek , such as the memory type and word width, into Insenser so that the programmable non-volatile memory of Furtek could be recognized by Insenser in order to enhance the storage adaptability, and for the above reason provided a motivation.

35. As to other limitations in claims 17,18,25, Insenser also taught at least one block of digital blocks being coupled to at least one analog circuit block (see any point of the digital blocks probed with the analog subsystem in col.3, lines 42-44)., wherein the digital circuit block were coupled to the analog circuit blocks (see inside blocks in fig.1 (3)14)), and at least one second digital block and analog block was coupled to microprocessor (see how the microprocessor read and write to analog and digital circuit blocks in col.3, lines 38-42, lines 45-47, see also how the lookup table mapped the functional blocks in col.4, lines 26-36, see also the inside functional blocks of analog subsystem (4) in col.4, lines 38-51).

36. As to the feature of the analog functional block is dynamically configurable and programmable, Insenser clearly taught his analog blocks was "programmable" and many functional parameters could be "configurable" (see col.4, lines 40-42). The fixed

functionality blocks were directed to the functionality blocks of coarse granularity, and it did not mean that Insensers analog functional blocks were not programmable and non-configurable.

37. As to the dynamically configurable and programmable digital block, Insenser's digital black was also dynamically configurable and programmable (see programmable digital cells in col.3, lines 15-19, see the microprocessor was used to reconfigure the cells in col.3, lines 45-46).

38. Insenser also included a plurality of analog functions (see the inside functional blocks of analog subsystem (4) in col.4, lines 38-51).

39. As to the single register write operation, neither Insensers nor Furtek specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). See reasons for obviousness above.

40. As to claim 20,21 , Insenser did not explicitly show the third digital circuit block was coupled to the fourth analog block as claimed. However, since Insenser already taught any point of the digital circuit blocks could probed with the analog circuit (see col.3, .lines 41-44), and that the system let user build a custom made application out of these circuit blocks (se col.4, lines 45-51), the examiner believes that any particular order, or pair, of connection between the digital blocks and analog blocks was possible through the reconfigurable system, and furthermore, no particular advantage of the third

digital block coupled to the fourth analog block is being reflected into the claim, therefore, it is viewed as any third digital block and any fourth analog digital block connection. Insenser did have the third digital circuit block (see any third inside blocks in fig.1 (3)), and a fourth analog block (see one of plurality of functional blocks in col.4, lines 38-46, see also the routing channels in col.3, lines 29-30, col.5, lines 5-1 1).

41. As to claim 26, Insenser's 1/0 also sent signals to microprocessor (see col.4, lines 52-53).

42. As to claim 27, Insenser also included plurality of 1/0 blocks with the digital and analog block (see the interconnection between the (7)(8) and (3)(4) in fig.1).

43. As to claim 28, Insenser also included a second 1/0 (8) connected to at least one analog blocks (see fig.1).

44. As to claim 29, see interconnection between digital blocks (3) and analog blocks (4).

45. As to claim 30, Insenser also include a connection between a third 1/0 (6) and the memory (1) (see fig.1).

46. As to claims 31 ,32, Insenser also included a plurality of registers and latches for storing programming data for the digital and analog circuit blocks (see the FF's in col.4, lines 21-36, see also fig.2).

47. As to the features of "microcontroller " and the " programmable non-volatile memory coupled to the digital blocks and analog blocks for programming " in claims 35,42, see discussions set forth above.

48. As to other limitations of claims 35,42, Insenser disclosed :

a) a plurality of 1/0 circuit blocks (see fig.1 (5)(6)(7)(8)(10));

b) a plurality of programmable analog circuit bocks (see the inside functional elements in fig.1 (4)) ;

c) a plurality of programmable digital circuit blocks (see the array of digital blocks in fig . 1 (3));

The plurality of 1/0 circuit blocks connected to the plurality of programmable analog circuit bocks the plurality of programmable digital circuit blocks (see interconnections in fig-l).

49. As to the feature of the analog functional block is dynamically configurable and programmable, Insenser clearly taught his analog blocks was "programmable" and many functional parameters could be "configurable" (see col.4, lines 40-42). The fixed functionality blocks were directed to the functionality blocks of coarse granularity, and it did not mean that Insensers analog functional blocks were not programmable and non-configurable.

50. As to the dynamically configurable and programmable digital block, Insensers digital black was also dynamically configurable and programmable (see programmable digital cells in col.3, lines 15-19, see the microprocessor was used to reconfigure the cells in col.3, lines 45-46).

51. As to the single register write operation, neither Insensers nor Furtek specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all

functional blocks or devices (see col.10, lines 30-38). See reasons for obviousness set forth above.

52. As to claim 36, Insenser's 1/0 also sent signals to at least a first one of the plurality of analog circuit blocks, and the analog sent to different one of the 1/0 blocks (see the communication connection between either (5)(6)(7)(8) or (10) to (4) in fig.1).

53. As to the routing matrix in claim 42, Insenser did not specifically show the routing matrix for coupling the subsets or plurality of analog and digital blocks as claimed. However, Furtek disclosed a global and macro routing matrix for coupling subsets of digital and analog blocks (see the routing of the signals in the partitioning of the matrix cells in col.5, lines 10-22, see also the logic circuit cells intersections with the function elements 83 as digital and analog circuit blocks in col.1 1, lines 60-66) . It would have been obvious to one of ordinary skill in the ad to use Furtek in Insenser for including the global or macro routing matrix as claimed because the use of Furtek could extend the processing structure of Insenser to accept additional macro blocks of the circuit, and because Insenser did disclose a large granularity of programmable cells (see col.4, lines 15-21), which was an indication of the need of a global or macro routing matrix into the system in order to manage great number circuit blocks in macro or global level, and in doing so, provided a motivation.

54. As to the feature of the analog functional block is dynamically configurable and programmable, Insenser clearly taught his analog blocks was "programmable" and many functional parameters could be "configurable" (see col.4, lines 40-42). The fixed

functionality blocks were directed to the functionality blocks of coarse granularity, and it did not mean that Insensers analog functional blocks were not programmable and non-configurable.

55. As to the single register write operation, neither Insensers nor Furtek specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). See reasons for obviousness set forth above.

56. As to digital function in claim 44, see Insensers col.6, lines 6-18.

57. As to claims 43,45, see plurality of analog functions in col.4, lines 37-43).

58. As to claim 46, Furtek's routing matrix also included the connection of the second subset often analog and digital circuit blocks (see the second matrix partitions in col.5, lines 4-22, se also the digital and analog cells in col.1 1, lines 60-67).

59. As to claim 47, Furtek also included M x N macros (see the matrix 4 x 4 in col.5, lines 2-18, see also the analog circuit cells in col.1 1, lines 60-67, se also fig.12).

28. As to claim 48, see the analog and comparator functions in col.1 1 , lines 60-67 in Furtek, see also the analog functions in col.4, lines 37-51 in Insenser).

60. As to claim 49, Insenser's digital blocks were connected in series (see fig.1 , first row 3)).

61. As to claim 51 , Insenser also included at least three digital blocks (see fig.1 (3)) connected in series and or parallel (see the row or column connections of three blocks

in (3J), controlled by lookup table (LUN including a cascade bit (see the LUT and cascade bits in col.4, lines 15-36) for determining the adjacent circuit blocks (see the 16 x 4 memory, the next bit position had to be an adjacent location or block, for example, 0001 is next to 0000 in the memory).

62. As to the single register write operation, neither Insensers nor Furtek specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). It would have been obvious to one of ordinary skill in the art to use van der Wal in Insensers for reconfiguring the digital functions with a single register write operation as claimed because the use of van der Wal could provide Insensers the ability to control the reconfigurable function blocks in a single integrated format, therefore, reducing the hardware circuit overheads, and it could be achieved by predefining the single register write of van der Wal into eh configuration file of Insensers with modified control variables (e.g. the instruction format, the write length etc.) so that the single register write of van der Wal could be recognized by Insensers, and because Insensers also taught a single microprocessor command for reconfiguring the SOC system (see col.5, lines 1-9), which was a suggestion of the applicability of a single register write operation in order to achieve specific register access operation for reconfiguring purpose, and for doing so, provided motivation.

63. As to claim 52, Insenser disclosed :

a) a micro controller (see fig.1 (2))..,

b) a subsystem comprising a functionalitypll4)

coupled to the microcontroller (see fig . 1 (3)(4));

c) coupling mechanism (see the reconfiguration tools in col.3, lines 45-612), wherein selectively, the functionality was configured to execute a first function according to a first input (see the configured programmable digital or analog cells), and implement a connection state (map, routing, placement) for the system by which the system was connectable to external entity (external devices) according to a second input (interface 7) (see col.3, lines 14-25).

64. Insenser also included first sub-functionality (digital function 3) and second sub-functionality (analog 4), wherein the interconnection mechanism was configured to interconnect the first sub-functionality digital function 3) and second sub- functionality (analog 4) according to a user input of third type (see CAD tools for configuring the programmable cells in col.3, lines 45-61).

65. As to the single register write operation, neither Insensers nor Furtek specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). It would have been obvious to one of ordinary skill in the art to use van der Wal in Insensers for reconfiguring the digital functions with a single register write operation as claimed because the use of van der Wal could provide Insensers the ability to control the reconfigurable function blocks in a single integrated format, therefore, reducing the hardware circuit overheads,

and it could be achieved by predefining the single register write of van der Wal into eh configuration file of Insensers with modified control variables (e.g. the instruction format, the write length etc.) so that the single register write of van der Wal could be recognized by Insensers, and because Insensers also taught a single microprocessor command for reconfiguring the SOC system (see col.5, lines 1-9), which was a suggestion of the applicability of a single register write operation in order to achieve specific register access operation for reconfiguring purpose, and for doing so, provided motivation.

66. As to claim 57, Insenser also included time bases according to user input (see the operating frequencies in col.4, lines 40-44, it was user input because it was programmable).

67. Furtek also disclosed a selected group of micro controllers (DFE) and other integrated circuits (programmable circuit cell 11) (see figs.12 , col.5, lines 3-29, col.1 1 , lines 56-65 for the DFE 83 as micro controllers and each of the partitions of programmable logic cells 11).

68. As to claims 33,34, Insenser did not specifically show the global or macro routing matrix for coupling the subsets or plurality of analog and digital blocks as claimed. However, Furtek disclosed a global and macro routing matrix for coupling subsets of digital and analog blocks (see the routing of the signals in the partitioning of the matrix cells in col.5, lines 10-22, see also the logic circuit cells intersections with the

function elements 83 as digital and analog circuit blocks in col.1 1, lines 60-66) . It would have been obvious to one of ordinary skill in the art to use Furtek in Insenser for including the global or macro routing matrix as claimed because the use of Furtek could extend the processing structure of Insenser to accept additional macro blocks of the circuit, and because Insenser did disclose a large granularity of programmable cells (see col.4, lines 15-21), which was an indication of the need of a global or macro routing matrix into the system in order to manage great number circuit blocks in macro or global level, and in doing so, provided a motivation.

69. As to the digital circuit blocks in claim 44, Insenser's digital functions. (e.g. see col.6, lines 6-18),

70. As to claims 43,45, see plurality of analog functions in col.4, lines 37-43.

71. As to claim 46, Furtek's routing matrix also included the connection of the second subset often analog and digital circuit blocks (see the second matrix partitions in col.5, lines 4-22, se also the digital and analog cells in col.1 1, lines 60-67).

72. As to claim 47, Furtek also included M x N macros (see the matrix 4 x 4 in col.5, lines 2-18, see also the analog circuit cells in col.1 1, lines 60-67, se also fig.12).

73. As to the amended claim 37, amended claim 37 is now rejected based on a new ground . Furtek is used to supplement the teaching of non-volatile memory. Insenser disclosed a plurality of programmable digital circuit blocks (see fig.1 (3)) including a microcontroller comprising ;

b) a plurality of analog circuit blocks (see fig.1 (4), see the plurality of analog functional blocks in col.4, lines 37-51).

c) a memory connected to the plurality of digital and analog circuit blocks (see fig.1).

74. Insenser did not explicitly show his analog and digital circuit blocks received first subset of programming data and second subset of programming data , respectively, as claimed. However, Insenser , in the same patent , disclosed a microprocessor was able to read the stored programming data (e.g. the two configuration contexts) for both the digital circuit and analog circuits (see col.2, lines 51-59). The source for storing the programming data (configuration contexts) was not clearly shown, but the examiner believes it had to be from the memory because the microprocessor had to be reading or writing into memory , therefore, since no other memory being presented by Insenser, the fist programming data (configuration) for the analog and second programming data (configuration) for the digital circuit had to be received from the memory based on the microprocessor read write command (see also col.4, lines 1-3).

75. As to the feature of non-volatile memory, Insenser did not specifically showed the non-volatile memory as claimed. However, Furtek disclosed a non-volatile memory (see col.12, lines 3-6). It would have been obvious to one of ordinary skill in the art to use Furtek in Insenser for including the non- volatile memory as claimed because the use of Furtek could provide Insenser the ability to adapt to different type of memory storage, and therefore, increasing the storage adaptability of Insenser, and it could be readily achieved by predefining the control parameters of the non-volatile memory of Furtek , such as the memory type and word width, into Insenser so that the non-volatile

memory of Furtek could be recognized by Insenser in order to enhance the storage adaptability, and for the above reason provided a motivation.

76. As to claims 38-41, Insenser did not explicitly show the connections of the particular ones of the circuit blocks (e.g. the second one of the analog circuit block) as claimed. However, since Insenser already taught any point of the digital circuit blocks could probed with the analog circuit (see col.3, .lines 41-44), and that the system let user build a custom made application out of these circuit blocks (se col.4, lines 45-51), the examiner believes that any particular order, or pair, of connection between the digital blocks and analog blocks was possible through the reconfigurable system (see also the routing channels in col.3, lines 29-30, col.5, lines 5-11).

77. Claims 58,59 are rejected under 35 U.S.C. 103(a) as being unpatentable over

78. Insenser (6,460,172) in view of Gammal et al. (5,754,826) in view of van der Wal et al. (6,188,381).

79. Insenser disclosed :

a) microcontroller (see fig.1 (2), col.3, lines 14-25),.

b) a subsystem coupled to the microcontroller comprising a plurality of analog functions and digital functions that were both configured by user input ICAD) (see fig.1, col.3, lines 37-61);

c) an interconnection (see the routing channels, interaction) configurable for selectively interconnecting the plurality of analog and digital functions according to user input (see fig.1, see the reconfigurable programmable cells in col.3, lines 45-61, see the programmable analog cells and digital cells in col.3, lines 14-24),

d) a coupling mechanism coupled to the subsystem that was configurable to implement connection state for system by which the system was connectable to external entity according to user input (see the external interface I8J in fig.1);.

e) selecting the functions and the interconnection state (see the reconfigurable programmable cells by the CAD tools in col.3, lines 45-61 , see the routing and placement for the interconnection state;

f) selecting the connection state (configuration) to effectuate a connection between the system and external entity correspond to a function (see either external interface 7 or 8 in fig.1, see also col.4, lines 61-65 for example of PC connection).

80. Although Insenser showed a plurality of analog and digital and mixed functions (see fig.1 (3)(4), see mixed signal for mixed digital and analog functions in col.3, lines 55-56), it did not specifically show a list of the analog and digital functions exactly as claimed. However, Gammal disclosed a netlist (see fig.3) including a plurality of functional cells (see the netlist for the symbolic representation in col.2, lines 17-26 for background, see col.6, lines 17-38 for the selected macro cells in the list). It would have been obvious to one of ordinary skill in the art to use Gammal in Insenser for including the list of he functionalities as claimed because the use of Gammal could provide Insenser the ability to control the plurality of the functional cells in a predetermined set

of program sequence, such as a netlist, thereby enhancing the connectivity of functional cells in a given format in the system , and because Insenser also taught the mapping and the library functions of the programmable cells which was an indication of the applicability of a list of the functional cells in the system in order to provide the enhanced programmable scheme , and in doing so, provided a motivation. Insenser is used as primary reference because it showed clearly the interconnection a microcontroller with the analog and digital functional cells. Gammal is used as secondary reference because it showed clearly the particular use of the functional cell netlist .

81. As to the feature of dynamically configurable and programmable analog blocks for providing various functions in claim 50, Insenser clearly taught his analog blocks was "programmable" and many functional parameters (i.e. the various analog functions) could be "configurable" (see col.4, lines 40-42). The fixed functionality blocks were directed to the functionality blocks of coarse granularity, and it did not mean that the analog functional blocks were not programmable and non- configurable (see also the microprocessor was used for reconfiguring the cells in col.3, lines 45-47).

82. As to the single register write operation, neither Insensers nor Gammal specifically showed single register write operation as clamed. However, van der Wal taught a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices (see col.10, lines 30-38). It would have been obvious to one of ordinary skill in the art to use van der Wal in Insensers for reconfiguring the digital functions with a single register write operation as claimed because the use of

van der Wal could provide Insensers the ability to control the reconfigurable function blocks in a single integrated format, therefore, reducing the hardware circuit overheads, and it could be achieved by predefining the single register write of van der Wal into eh configuration file of Insensers with modified control variables (e.g. the instruction format, the write length etc.) so that the single register write of van der Wal could be recognized by Insensers, and because Insensers also taught a single microprocessor command for reconfiguring the SOC system (see col.5, lines 1-9), which was a suggestion of the applicability of a single register write operation in order to achieve specific register access operation for reconfiguring purpose, and for doing so, provided motivation.

83. As to claim 59, Insenser also included a plurality of time bases (see the operating frequency of the filters in col.4, lines 41-44).

Ahy inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

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21 Century Strategic Plan